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AN11685

Recommendations for printed circuit board assembly of DSN0402 (SOD992)

Rev. 1 — 5 January 2016 Application note

Document information

Info	Content
Keywords	DSN0402, SOD992, 01005 package size, reflow soldering, Surface-Mounted Device (SMD), solder paste, stencil aperture, Printed-Circuit Board (PCB), footprint, landing pattern, pick and place, Chip Scale Package (CSP)
Abstract	This application note provides guidelines for board assembly of the ultra-small DSN0402 (0.4 × 0.2 mm^2) chip-scale package. The main focus is on recommendations for reflow soldering. For general information about footprint design and reflow soldering see application note AN10365 (Surface mount reflow soldering description).

Revision history

Rev	Date	Description
1	20160105	Initial version

Contact information

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1. Introduction

With the trend of reduced dimensions and increased density of functionality in smart phones and other mobile devices, there is rising demand from the industry for extremely small components. The new DSN0402 (SOD992) package with only 0.4 mm x 0.2 mm x 0.12 mm (01005) supports this trend. NXP offers an ultra-small surface mount chip scale diode package.

Due to the very small size of the component, NXP investigated the board assembly process intensively in order to offer board mounting recommendations.

These recommendations include PCB mounting pads, stencil apertures, solder paste and board assembly process parameters.

Using the recommended dimensions for pads and stencil as described in this document help to achieve:

- optimum stand up height
- minimum tilt
- minimum rotation
- good board assembly process performance
- optimum board level reliability

While this application note should help minimizing any unexpected failures, following the advice in this document is not a guarantee for a perfect SMT assembly result. The results may differ depending on the machine capability, ambient conditions and material.

2. DSN0402 (SOD992) package details

The DSN0402 (SOD992) is a Discrete Silicon No Lead package (DSN). It features tin (Sn) plated metal contacts under the package (bottom terminations) similar to DFN style packages. The DSN style package allows 100% utilization of the package area for active silicon. It is offering a significant performance advantage per board area compared to products in plastic molded packages.

The new production technology of the DSN0402 results in very accurate dimensions with a tolerance of only ±10 μm. The package comes with an extremely low overall height of 120 μm only.

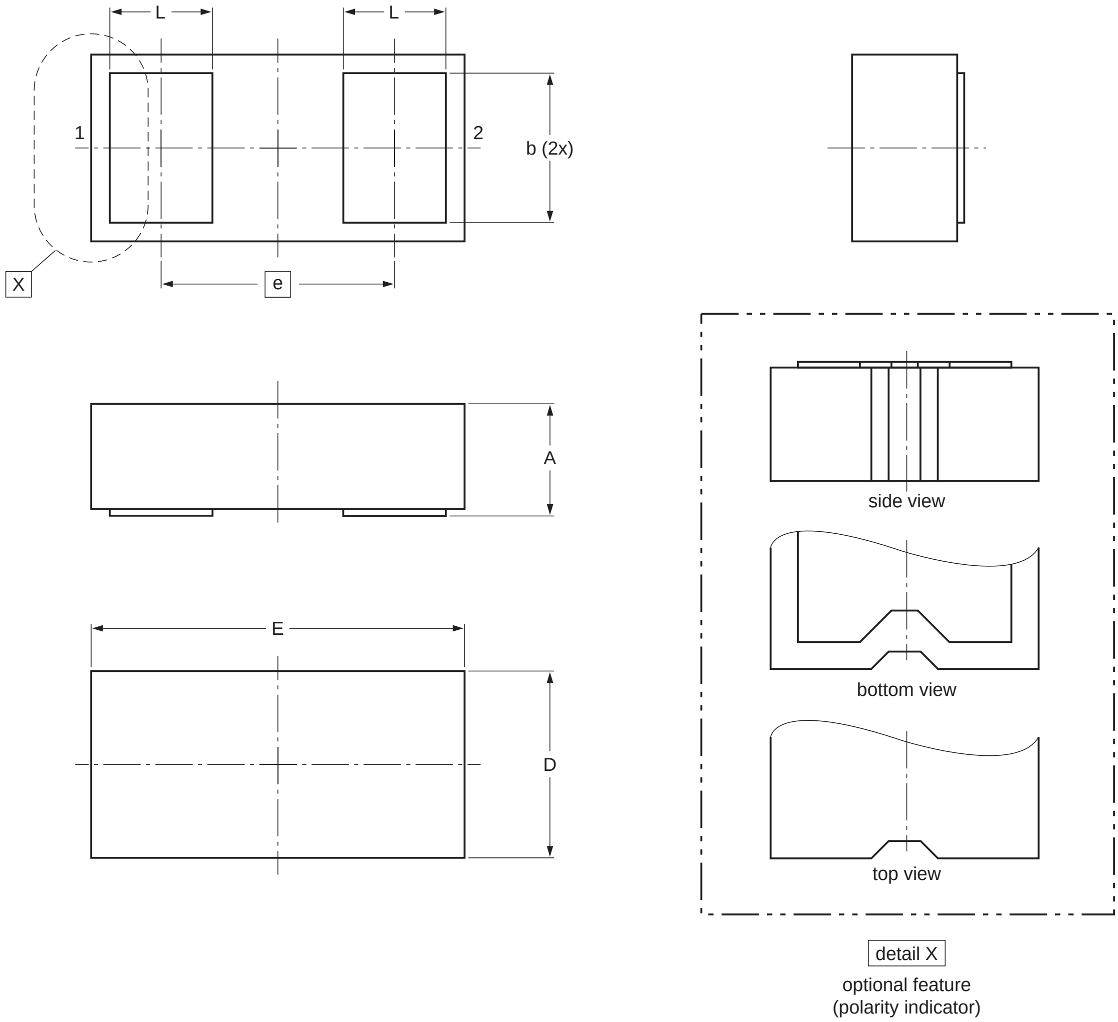
Key Features:

- Ultra small and flat package ($0.4 \times 0.2 \times 0.12$ mm^3)
- The package area is 45% of the DSN0603 (SOD962)
- Ultra low dimensional tolerances of ±10 μm
- Sn-plated contacts for soldering on PCB
- No package internal interconnects like wire bond of flip chip (beneficial to minimize impedance)
- Side wall coating which provides some protection against environmental factors, such as humidity, contamination, solder paste and flux
- Polarity marking visible from top and bottom (not applied for symmetric bidirectional diodes) enables optical polarity check by pick and place machines and on PCB

Remark: Bidirectional type without polarity indicator (notch)

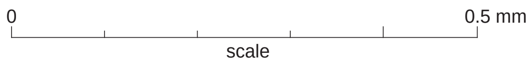
Fig 1. DSN0402-2 (SOD992): visual appearance

DSN0402-2, leadless tiny package; 2 terminals **SOD992**



Dimensions (mm are the original dimensions)

Unit		A	E	D	L	b	e
mm	max	0.14	0.41	0.21	0.12	0.17	
	nom	0.12	0.40	0.20	0.11	0.16	0.25
	min	0.10	0.39	0.19	0.10	0.15	



sod992_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOD992						~~13-11-07~~ 15-08-25

Fig 2. DSN0402-2 (SOD992): package dimensions

3. PCB solder pattern

3.1 Solder pad design: general options

There are two types of solder pad / solder resist designs:

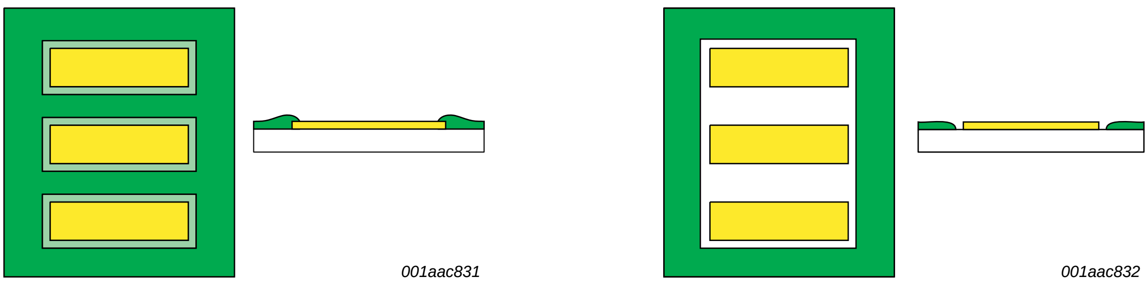
Solder Mask Defined (SMD) and Non-Solder Mask Defined (NSMD).

SMD is a method of designing the solder resist to partially overlap the copper (Cu) landing pattern on the PCB. NSMD designs have a gap between the solder resist and the Cu landing pattern on the PCB. These two types are described in more detail in the next chapter.

3.1.1 SMD solder pad versus NSMD solder pad

If the solder mask extends onto the solder lands, the remaining solderable area is Solder Mask Defined (SMD). The effective solder pad is equal to the copper area, that is not covered by the solder mask. This situation is illustrated in Figure 3, left column. In case of an SMD pad, the copper normally extend 75 μm down to 50 μm underneath the solder mask on all sides. In other words, the copper dimension is 0.1 mm to 0.15 mm larger than the solder mask dimension. These values may vary depending on the class of PCBs are used. This measure allows tolerances in copper etching and solder mask placement during PCB production.

Non-Solder Mask Defined (NSMD) is given, when the solder mask layer starts outside of the solder lands and does not cover the copper. The effective solder pad is equal to the copper area. In case of an NSMD, the solder mask should be at least 50 μm away from the solder land on all sides. In other words, the solder mask dimension is 100 μm larger than the copper dimension. These values may vary depending on the class of PCBs used. The main requirement is that the solder mask is sufficiently far away from the copper. With the given tolerances in solder mask application, the mask may not extend onto the copper. An NSMD footprint is shown in Figure 3, right column.



a. SMD solder pad   b. NSMD solder pad

Fig 3. Solder Mask Defined (SMD) versus Non-Solder Mask Defined (NSMD) solder pads

3.2 Solder pad design for DSN0402 packages (SOD992)

3.2.1 Recommended reflow solder footprint

Based on the small dimensions of 0402 (01005) devices and the given tolerances for PCB manufacturing, NXP recommends using Non-Solder Mask Defined (NSMD) solder pads. Especially the gap between the CU pads (with the PCB design tolerances) is with 140 μm small for a reasonable solder resist trace. In addition, such a resist trace would cause a higher tendency for tilting/rotation. Therefore, the recommended solder footprints are NSMD pads.

The solder footprint with dimensions and the solder footprint together with the package outline are shown in Figure 4 and Figure 5.

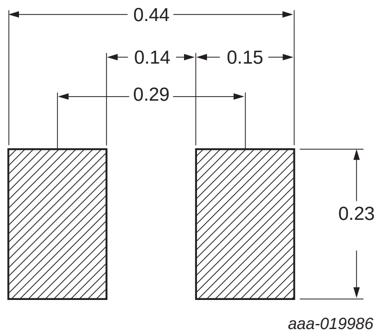


Fig 4. DSN0402-2 (SOD992): recommended reflow solder footprint

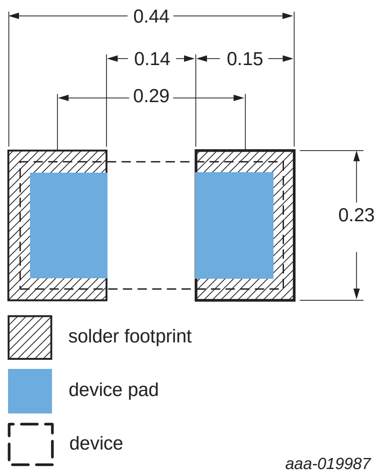


Fig 5. DSN0402-2 (SOD992): recommended reflow solder footprint with package outline

3.2.2 Smallest Reflow Solder Footprint Design

The size of the solder pads as shown in Figure 4 and Figure 5 have also been optimized for a reasonable stencil aperture (refer to Section 4). In case a higher device density on PCB is required, it is possible to use smaller footprints. The sizes of the footprints equal to the device pad sizes. These layouts are shown in Figure 6 and Figure 7. The disadvantage is that the appropriate stencil aperture would be too small for a reasonable area ratio (refer to Section 4.2, Table 1 and Table 2). Here a high-quality stencil and high control effort for the printing process is necessary. Even with high effort the solder paste volumes might be unstable as a result of the printing process.

Another aspect to achieve the best possible soldering result was found within the investigations:

The device tilting and/or rotation can be minimized if the relation of stencil aperture versus solder pad size is kept in ratio of < 1 (as for the recommended solder layout, refer to Figure 16).

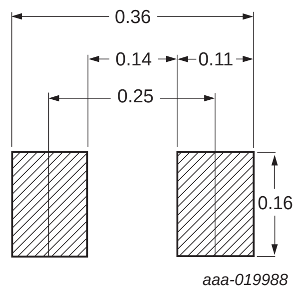


Fig 6. Reflow solder footprint size equals device pad size

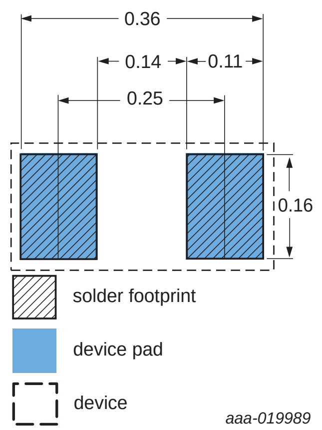
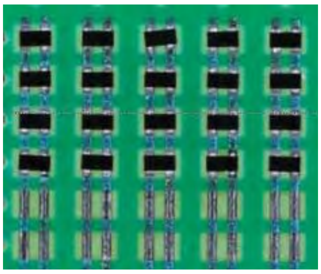


Fig 7. Reflow solder footprint with package outline

3.2.3 Route-through solder footprint consideration

Connection by route-through was also included in the soldering investigations. Route-through design in this case refers to a continuous CU trace covered by solder resist which is removed only at the solder pad positions. For illustration, refer to Figure 8. Due to the tolerances of the solder resist lithography, the openings have to be relatively large so that solder paste printing and component placement fit together.
Due to this large solder mask clearance, the DSN0402 packages have a tendency for undefined tilting and/or rotation. For these reasons, a route-through solder footprint design is not preferred.



aaa-019990

Fig 8. Route through solder pad design example

3.3 NXP DSN0402 (SOD992) on competitor footprint

The NXP DSN0402 has a coating on the side walls which mitigates leakage current rejects caused by flux and solder. Due to this coating, it is possible, to place the devices on solder footprints with limited deviation from NXP recommendation (refer to chapter 3.2.1). Beware that the soldering result in terms of tilting and/or rotation may not be optimal. The footprints as shown in Figure 9 and Figure 10 have been evaluated. The soldering results of NXP DSN0402 on these footprints are good.

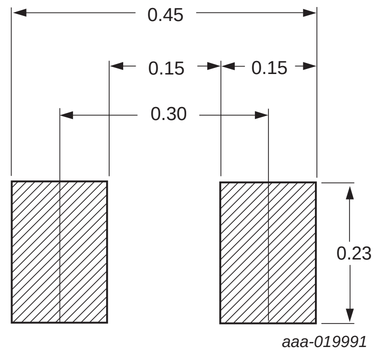


Fig 9. Competitor reflow solder footprint as evaluated for NXP DSN0402

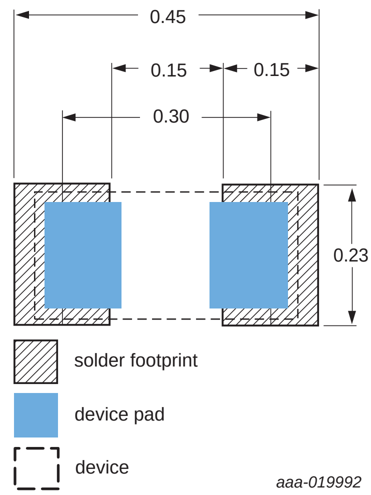


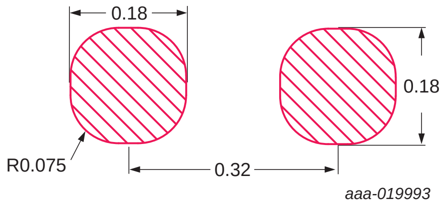
Fig 10. Competitor reflow solder footprint and package outline as evaluated for NXP DSN0402

4. Solder Stencil

4.1 Stencil Recommendations

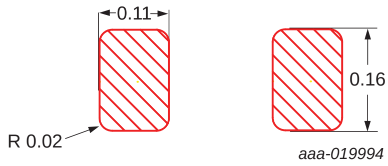
Due to small apertures and pad dimensions, a high-quality stencil should be used. NXP used a stainless steel stencil, manufactured by laser-cut and with plasma coating for investigation. A nano-coated stencil showed an even better release performance at solder paste printing.

For the recommended NXP footprint (see Section 3.2.1, Figure 4 and Figure 5), the optimum stencil aperture is of size 0.18 x 0.18 mm^2. Based on the experience of stencil manufacturers, rounded corners with a radius of 0.03 mm are sufficient for a good solder paste release during printing. In order to reduce the solder volume, a radius of 0.075 mm was realized for the NXP solder footprint. For investigated stencil apertures, refer to Figure 11, Figure 12 and Figure 13.



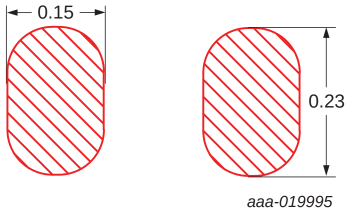
Area ratio at T = 80 µm: 0.56

Fig 11. NXP recommended aperture



Area ratio at T = 80 µm: 0.41

Fig 12. Aperture size same as device pad size



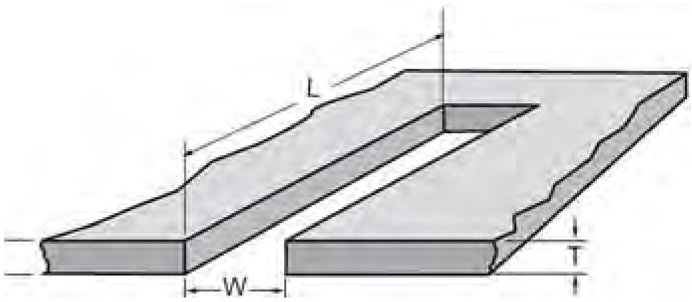
Area ratio at T = 80 µm: 0.59

Fig 13. Investigated competitor aperture recommendation

4.2 Stencil aperture design

Key design guidelines for stencil apertures are the area and aspect ratios. The area ratio for a standard approach is >0.66. Ultra-small devices like DSN0402 need a smaller ratio to achieve optimum assembling reliability. Smaller values are possible with adequate process control. These small values depend on the manufacturing environment and other requirements of the manufacturer.

The aspect ratio should be >1.5 which is less critical to fulfill. For explanation of area and aspect ratio, refer to Figure 14.



Cross -sectional view of a stencil

aaa-019083

$$\text{Area ratio} = \frac{\text{area of aperture opening}}{\text{area of aperture walls}} = \frac{L \times W}{2 \times (L + W) \times T}$$

$$\text{Aspect ratio} = \frac{\text{width of the aperture}}{\text{thickness of the stencil foil}} = \frac{W}{T} > 1, 5$$

Fig 14. Explanation of area and aspect ratio

Table 1. Area and Aspect Ratio for stencil apertures as investigated

Stencil thickness T = 80 μm

	Aperture size	Area ratio	Aspect ratio
NXP recommended footprint	180 × 180 μm^2	0.56	2.25
Footprint equals device pad size	160 × 110 μm^2	0.41	1.38
Competitor footprint	230 × 150 μm^2	0.59	1.9

Table 2. Area and Aspect Ratio for stencil apertures as investigated

Stencil thickness T = 100 μm

	Aperture size	Area ratio	Aspect ratio
NXP recommended footprint	180 × 180 μm^2	0.45	1.8
Footprint equals device pad size	160 × 110 μm^2	0.33	1.1
Competitor footprint	230 × 150 μm^2	0.47	1.5

Table 1 shows the values for aspect and area ratio of the considered stencil apertures for a stencil thickness of 80 μm. It results in an area ratio of 0.56 for the NXP footprint recommendation. For such small areas, the radius of the aperture should be considered for the calculation. Doing so the area ratio increases to 0.58 by considering the radius of 75 μm. In case of reduction to 75 μm stencil thickness, an area ratio of 0.60 (0.62 with considering the 75 μm radius) can be achieved for the NXP recommended stencil aperture. The minimal solder footprint dimension is only feasible in case of advanced process control.

In Table 2, the values for aspect and area ratio for a 100 μm thick stencil are listed. The minimal footprints are surely not recommended any more for a 100 μm stencil thickness. The footprints may work in a tightly controlled process (with help of 3D solder print inspection). In addition to the stencil design guidelines, the potential device tilting also needs to be considered as a result of relatively high solder past volumes and variation in printing. NXP does not recommend using a stencil thickness > 80 μm.

5. Solder Paste

Besides stencil aperture and thickness, the used solder paste has a significant impact on the printing performance. Solder pastes are available in different solder powder grain sizes. Refer to Table 3.

Table 3. Survey of solder paste types (grain sizes)

Type	Less than 0.5%, larger than	10% max between	80% min between	10% max less than
1	160	150 - 160	75 - 150	75
2	80	75 - 80	45 - 75	45
3	60	45 - 60	25 - 45	25
4	50	38 - 50	20 - 38	20
5	40	25 - 40	15 - 25	15
6	25	15 - 25	5 - 15	5
7	15	11- 15	2- 11	2

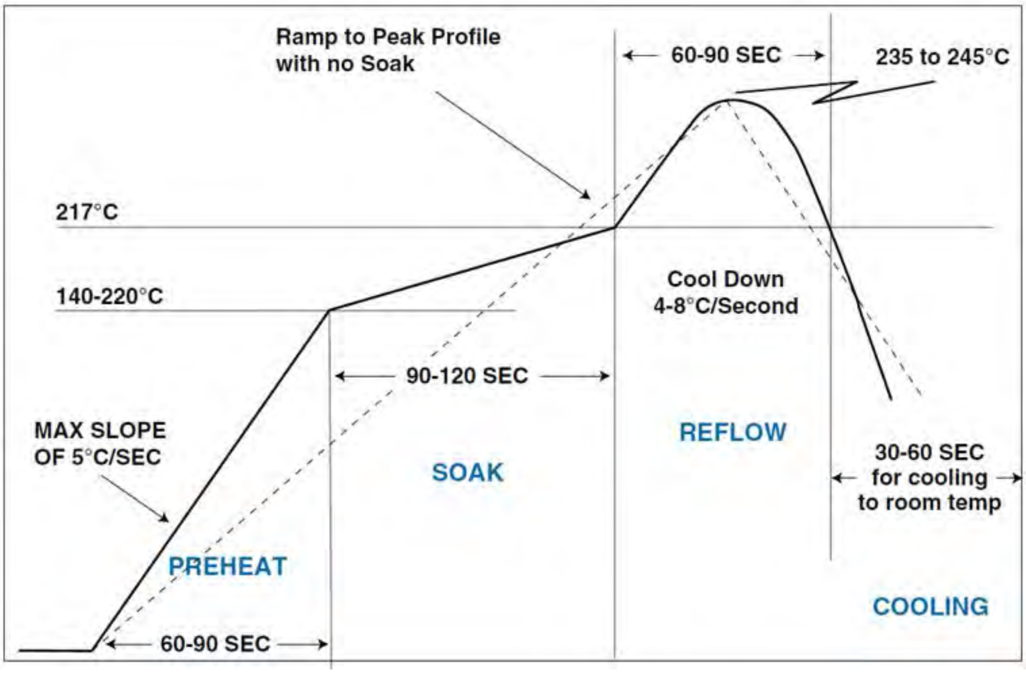
Solder paste type 4 and 5 were used for investigations with different solder pad and stencil apertures for the DSN0402 (SOD992) package. Best results were obtained with type 5 pastes in combination with 80 μm stencil thickness. Using type 4 solder paste tends to result in unstable solder volumes. For a reduction of the stencil thickness to 60 μm, it should be considered to use a type 6 solder paste.

6. Soldering Process

For soldering of DSN0402 packages, the following solder processes were considered:

- Convection reflow under nitrogen atmosphere is clearly preferred
- Convection reflow under air atmosphere also works, but
  - Using an unfavorable layout results with DSN0402 packages in leaning towards undefined placement (tilting, rotating, misplacement) and solder joints show a tendency of increased voiding
  - Solder joint surfaces are rough, flux residues often become darker and the soldering behavior may deteriorate
- Vapor phase soldering is also possible

For investigation of reflow soldering, a profile as recommended for SAC Alloys by IPC-7095 was applied. Refer to Figure 15.



Source: IPC-7095C

aaa-020015

Fig 15. Reflow solder profile as applied for investigation

7. Handling Recommendations

Besides the PCB and stencil design requirements, the ultra-small size and low weight of the DSN0402 requires attention to the Pick and Place (P&P) process. Electrostatic charge may cause problems during the pick and place (tape out) process. NXP has implemented preventive measures such as using a conductive plastic carrier tape (embossed tape) instead of a paper tape. Paper tape is commonly used for passive 01005 components. Also the cover tape is static dissipative. During extensive P&P trials, the following could be observed: A relative humidity below 30% in the production area leads to increased P&P (tape out) errors caused by electrostatic charging. Therefore, the environment should be controlled to >30% RH. In any case, the feeders should be carefully connected to ground to avoid electrostatic charging.

Another observation is that feeders of some P&P suppliers require inserts or springs below the carrier tape. For embossed carrier tapes of such small components, the inserts require a gap for the carrier tape pockets to achieve a smooth indexing without vibration. In this case, P&P machine suppliers should be contacted for recommendations.

For an optimum tape out yield, the cover tape peel off position should be as close as possible to the pick-up position of the devices. That measure prevents any rotation of products due to mechanical movement and vibrations. The risk of rotation was still observed even when the products had been covered by a metal plate after the cover tape was peeled off.

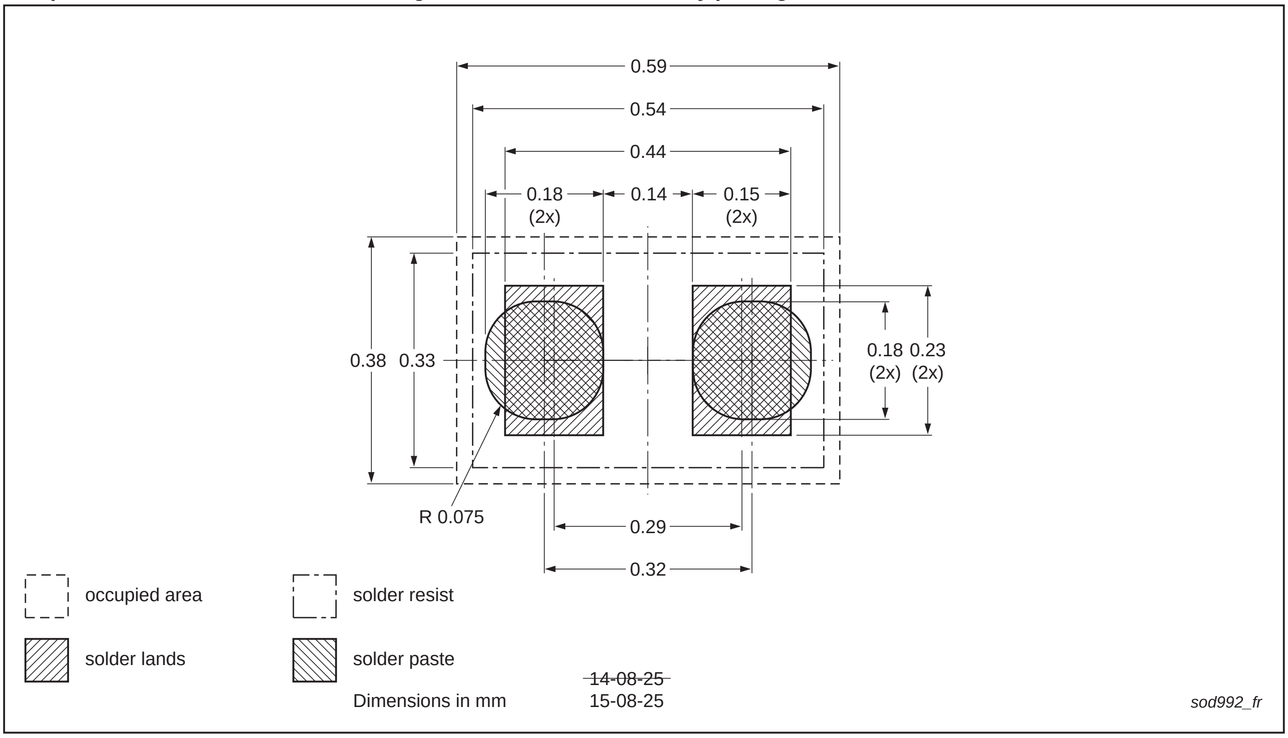
Manual handling by tweezers (for PCB repair) is strictly not recommended, as it would destroy the side wall coating and may also damage the silicon.

8. Summary

8.1 Recommended solder footprint and stencil aperture

The recommended solder footprint including stencil aperture is shown in Figure 16.

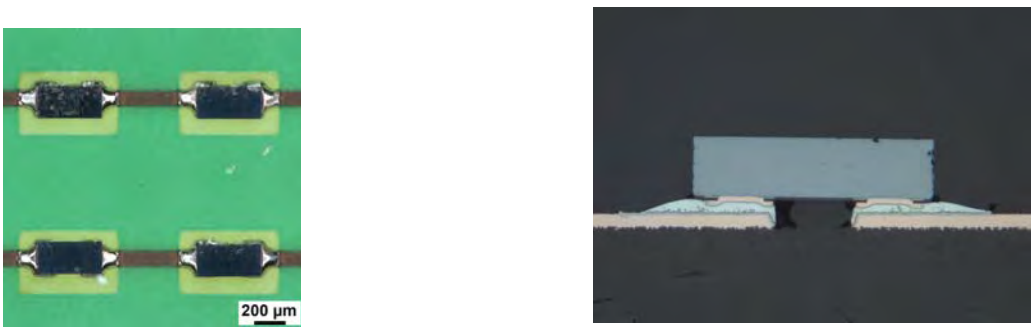
Footprint information for reflow soldering of DSN0402-2, leadless tiny package; 2 terminals **SOD992**



Recommended stencil thickness: 80µm

Fig 16. Solder footprint and stencil aperture

8.1.1 Real Device on recommended solder footprint



aaa-020025 *aaa-020026*

a. Top view b. Cross section

Fig 17. DSN0402 soldered on recommended footprint, paste T5, stencil T = 80 µm

8.2 Further recommendations

8.2.1 Stencil layout and solder paste

- Stencil thickness of 80 μm in combination with Type 5 solder paste (refer to Table 3) is recommended.
- A no-clean paste with a J-STD-004 classification “L0” is recommended.
- Stencil thickness of 100 μm might also work but is clearly not recommended because:
  - The products tend to tilt due to the high amount of solder paste.
  - The amount of printed solder paste tends to vary more compared to thinner stencils which makes the printing process unstable.
- A stencil aperture dimension as shown in Figure 11 and Figure 16 is recommended.
- To get best printing (and soldering) results, the cleaning cycle of the stencil should be carefully controlled.
- A stainless steel stencil, manufactured by laser-cut and with plasma coating should be used. Further print performance improvement is possible by usage of a nano-coated stencil.

8.2.2 Solder pad design

- NSMD pads with a gap between Cu pad and solder resist of 50 μm are recommended.
- Conductor (Cu trace) between solder pads on PCB is not recommended.
- Connection of solder pads by μVia is not recommended.
- Connection by Cu traces (lines) is preferred.
- Connection by route-through might also be possible, but due to a large solder mask clearance, DSN0402 packages show a tendency of tilting and rotation. With that route-through solder pads are not recommended.

8.2.3 Soldering process

- Convection reflow under nitrogen atmosphere is preferred.
- Convection reflow under air atmosphere also works, but
  - Using an unfavorable layout, products lean towards undefined tilting and rotation and solder joints show a tendency of increased voiding.
  - Solder joint surfaces are rough, flux residues often become darker and the soldering behavior may deteriorate.
- For ultra-small devices with two terminals like DSN0402, the convection airflow in the reflow oven should be considered, as it might cause tilting of devices.
- Vapor phase soldering is also possible.

8.2.4 Handling recommendations

- Manual handling with tweezers (for repair) is not recommended
- Feeders of P&P machines: In case inserts required underneath the carrier tape, a gap in this insert for the carrier tape pocket should be implemented. Some feeders require a spring underneath the carrier tape. The cover tape peel-off position should be as close as possible to the device pick-up position. A reduction of feeding speed can help to improve tape out yield. Ask P&P machine supplier for further recommendations.
- Feeders should be carefully connected to ground, in order to avoid electrostatic charging.
- Keep control of thawing time of solder paste bundle to avoid too much humidity in paste.
- Relative humidity of shop floor at solder paste print until reflow should be controlled to 40% to 60% to prevent drying of flux in solder paste.
- Relative humidity for P&P should be > 30%.

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10. Contents

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